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MENDELSON AND ASSOCIATES, P.C.			EXAMINER	
1500 JOHN F. KENNEDY BLVD., SUITE 405			PATHAK, SUDHANSU C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/727,450	Applicant(s) ADAMIECKI ET AL.
	Examiner SUDHANSU C. PATHAK	Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 May 2008.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-29 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-29 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 04 December 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1668)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____

5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

1. Claims 1-29 are pending in the application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.
3. In regards to the specific argument that "Claim 1 has been amended to distinguish the claimed invention over the cited references. In particular, according to currently amended claim 1, an original data signal is transmitted through an electrical backplane or through the electrical backplane and at least one filter. The original data signal is a binary data signal, and the transfer function property of the electrical backplane or the transfer function property of the combination of the electrical backplane and the at least one filter corresponds to the transfer function property of a binary-to-duobinary converter. The data signal is received after being transmitted through the electrical backplane or through the electrical backplane and the at least one filter, wherein the received data signal is processed as a duobinary data signal". This limitation is disclosed in the AAPA in view of new reference Ginzburg et al. (5,412,691) as described below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-10, 15 (method) & 18-24, 27 (system) & 29 (apparatus) are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Ginzburg et al. (5,412,691).

In regards to Claims 1, 3, 15, 18-19 & 29, the AAPA discloses a method (system/apparatus) of processing data signals (Specification, Page 1, lines 9-28) comprising: transmitting the data signal through an electrical backplane (Specification, Page 1, lines 9-20) {Interpretation: The reference discloses transmitting data over multi-layer board called high-speed backplane}. However, the AAPA does not disclose transmitting binary data signal; the transfer function property of the channel or the transfer function property of the combination of the channel and the at least one filter corresponds to the transfer function property of a binary-to-duobinary converter; and receiving the data signal after being transmitted through the electrical backplane or through the electrical backplane and the at least one filter, wherein the received data signal is processed as a duobinary data signal.

Ginzburg discloses a method for processing a data signal (Fig.'s 1, 2A-D), comprising: transmitting an original data signal (Fig. 1, element "Digital Input Signal") wherein: the original data signal is a binary data signal (Fig. 4, element "Binary Data In"); the transfer function property of the channel or the transfer function property of the combination of the channel and the at least one filter corresponds to the transfer function property of a binary-to-duobinary converter; and receiving the data signal after being transmitted through the electrical backplane or through the electrical

backplane and the at least one filter, wherein the received data signal is processed as a duobinary data signal (Abstract, lines 1-6, 11-15 & Fig.'s 1, 2A-D & Fig.'s 4, 5A-D & Column 1, lines 20-25, 39-45, 59-64 & Column 2, lines 22-33, 53-63 & Column 3, lines 48-58 & Column 4, lines 5-12, 58-68 & Column 5, lines 47-to-Column 6, lines 39 & Column 6, lines 58-68) {Interpretation: The reference discloses encoding binary data into duobinary data and further equalizing (filtering) the duobinary data so as to equalize the effects of the band-limited channel, thus the signal received is a duobinary encoded data. The process of equalizing is interpreted as filtering and this is performed in the transmitter thus the filtering is performed prior to receiving data}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Ginzburg teaches transmitting binary data signal; the transfer function property of the channel or the transfer function property of the combination of the channel and the at least one filter corresponds to the transfer function property of a binary-to-duobinary converter; and receiving the data signal after being transmitted through the electrical backplane or through the electrical backplane and the at least one filter, wherein the received data signal is processed as a duobinary data signal and this is implemented in the method of transmission of data over an electrical backplane as described in the AAPA so as to be able to perform equalization (filtering) in the transmitter at a lower cost. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a receiver to receive the encoded and equalized signal and further that

since the equalization perform the equalization of the channel the received signal is the encoded signal.

In regards to Claims 2, 16 & 27, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses precoding a binary data signal, wherein the data signal transmitted through the electrical backplane is based on the precoded binary data signal (Column 6, lines 14-25 & Fig.'s 5A-D). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim.

In regards to Claims 4-5, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses the filtering is implemented before transmission through the electrical backplane (Column 6, lines 58-62 & Column 1, lines 39-45 & Column 4, lines 64-to-Column 5, lines 1-2) {Interpretation: The reference discloses performing equalization (filtering) prior to transmission over the channel}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim.

In regards to Claims 6-7, 20, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses filtering is designed to emphasize high- frequency components in the data signal and flatten group delay of the electrical backplane (Column 1, lines 38-46 & Fig. 2C) {Interpretation: The reference discloses equalizing the effects of the band-limited

transmission channel in both frequency and phase thus inherently flatten group delay}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing an equalizer filter in digital domain is implemented using a FIR filter and this is implemented in the equalizer as described in Ginzburg so as to be able to implement a digital filter so as to be able to vary the parameters (filter characteristics) as desired by the user before the transmission of the data.

In regards to Claims 8 & 21-22, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses the filtering: delays a first copy of the data signal (Fig. 4, element 52); attenuates the delayed first copy (Fig.'s 1, 3, element 14) and adds the delayed first copy to a second copy of the data signal to generate the filtered data signal (Fig. 4, element 54). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim.

In regards to Claims 9 & 23, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses the combination of the filtering and the transmission through the electrical backplane approximates binary-to-duobinary conversion (Fig. 2A-D & Column 4, lines 59-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim.

In regards to Claim 10 & 24, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. Ginzburg further discloses the duobinary-to-binary (D/B) conversion is applied to the received data signal to generate an output binary data signal (Column 5, lines 60-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Ginzburg satisfies the limitations of the claim. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing a duobinary-to-binary conversion so as to recover the encoded (binary-to-duobinary) conversion at the transmitter.

6. Claims 11-14, 17 (method) & 25-26, 28 (system) are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Ginzburg et al. (5,412,691) and further in view of Murray et al. (GB 2,217,957).

In regards to Claims 11-14, 17 & 28, the AAPA in view of Ginzburg discloses a method (system) of processing data signals as described above. However, AAPA in view of Ginzburg does not disclose the D/B conversion comprises a splitter, comparing amplitude of the received data signal with first and second threshold voltages to generate first and second binary streams; and applying a logic function to the first and second binary streams to generate the binary data signal wherein the logic function comprises an exclusive-OR (XOR) or exclusive-NOR (XNOR) function and further the AAPA in view of Ginzburg does not disclose an NRZ binary data.

Murray discloses a D/B conversion comprising a splitter (Fig. 1) {Interpretation: The reference in Fig. 1, shows splitting the received signal and inputting the split signal into a plurality of diodes}; comparing amplitude of the received data signal with first and second threshold voltages to generate first and second binary streams (Fig. 1, elements "CP1" & "CP2"); and applying a logic function to the first and second binary streams to generate the binary data signal wherein the logic function comprises an exclusive-OR (XOR) or exclusive-NOR (XNOR) function (Fig. 1, element "G"). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Murray teaches D/B conversion comprises comparing amplitude of the received data signal with first and second threshold voltages to generate first and second binary streams; and applying a logic function to the first and second binary streams to generate the binary data signal wherein the logic function comprises an exclusive-OR (XOR) or exclusive-NOR (XNOR) function and this is implemented in the method as described in AAPA in view of Ginzburg so as to be able to decode the received duobinary signal. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that there is no criticality in implementing a NRZ data this is a matter of design choice and this is indeed implemented in the decoder as described in Murray.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUDHANSU C. PATHAK whose telephone number is (571)272-5509. The examiner can normally be reached on 9am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sudhanshu C Pathak/
Primary Examiner, Art Unit 2611